REMARKS

File History

In the latest substantive Office action of 8/05/2005, the following allowances, rejections, objections and other actions appear to have been made:

- Claims **1-10, 14, 16-35** were rejected under 35 USC §102(e) as being fully anticipated by **Douceur** (US 6,247,061 based on app filed June 9, 1998).
- Claims 11-13 and 15 were indicated to contain allowable subject matter relative to the applied art.
- Claims 1-35 were all rejected for indefiniteness pursuant to 35 USC §112 but no specific reasons were provided for why the USPTO so rejects these claims.
- The Title is objected to as not being descriptive.
- Insertion of missing cross reference numbers is requested.
- Submission of an Information Disclosure Statement (IDS) was suggested.

Summary of 10/11/2005 Conference with Examiner

Applicant thanks the Examiner for the courtesy of the telephone conference of Oct. 11, 2005. No agreements were reached with respect to allowability of any claims. The Examiner clarified the intent of the indefiniteness rejection, namely that it constitutes a request for more information regarding what concepts tie all the claims together. Applicant's representative briefed the Examiner on the independently clocked entities shown in Fig. 1A, the fast clock-slow clock rate creep problem and the time frame synchronization problem. It was agreed that Applicant would present these concepts in this response.

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Summary of 10/12/2005 and Subsequent Conferences with Examiner

Applicant thanks the Examiner for the courtesy of the telephone conferences of Oct. 12-26, 2005. Applicant submitted informal suggestions to the Examiner of where appropriate lines of restriction may lie, but no agreements were reached. The Examiner should note that Claim 36 of the present formal amendment is not completely the same as the version shown in the informal communications.

Summary of Current Response

Claims 36-44 are newly added.

The specification is amended.

Arguments are presented concerning the applied art and its proposed combination.

An IDS is submitted.

Notes on Co-related applications

As noted above, Ser. No. 09/846,875 issued as US Pat. 6,748,567 on June 8, 2004. As of this response date, Ser. No. 09/905,394 and 09/865,258 have been allowed. Allowed claims are indicated in Ser. No. 09/847,711, but the PTO is waiting for Applicant to cancel non-elected claims (and Applicant may submit additional claims therein).

Applicants' Overview of Outstanding Office Action

Applicant sees the outstanding Office action of 8/05/2005 as having the following major features:

(1) In summarily rejecting all the claims for indefiniteness, the examiner is actually *asking for an explanation* of what the claims mean. (See OA page 3, paragraph 10.) Applicant will try to clarify here, but without surrendering claim scope.

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(2) In rejecting Claim 1 for anticipation, no weight is given to the preamble despite the fact that the body of the claim makes antecedent reference to the preamble. The same appears true for others of the claims whose bodies make antecedent reference to their preambles.

(3) There is no discussion of the specifics of any claim *taken in whole* compared against specific elements and functions of the Doucere '061 reference. Instead, a sweeping conclusion is made that all of claims 1-10, 14, 16-35 are anticipated.

In view of the above, it is respectfully submitted that a prima facie case of unpatentability has not been made out.

Initial Remark On PTO's Request for Simplification

It is understandable to want simplicity. Simple concepts are easier to process than complex ones. Not everything can be simplified however without loss of comprehension.

Applicant takes the PTO's indefiniteness rejection at OA page 3 and the PTO's request for a more "descriptive" Title of Invention as constituting a request for help. Applicant will try to comply.

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In the top right corner of Fig. 1A, it is indicated that the number 1 "main concept" is:

(1) **CLOCK-FREE TREE SCALABILITY**

In plain English, what does that mean? It means that the system can be expanded (scaled) without having to grow a continuous clock tree as is necessary in synchronously operated digital systems. One can add an independently clocked expansion board to the system and yet have operations within the system synchronized to a specific time frame.

The illustrated system of Fig. 1A can be expanded by:

1) Adding an independently-clocked, data sourcing circuit (i.e., a new line card 110); or

2) Adding an independently-clocked, data processing circuit (i.e., a new switch card 160); and/or

3) Adding new serial interconnect lines in the serial interconnect fabric 103.

The reason other practitioners have not pursued clock-tree free scalabilty is because it creates a number of headaches. Chief among these are the outcomes that:

1) The added-on but *independently-clocked*, data processing and/or data sourcing circuit will be **out of time synch** with the rest of the system; and

2) Faster ones of the *independently-clocked* entities will outpace slower ones, leading to buffer overrun problems or the like. This problem is referred to as "**rate creep**" in the specification (and also at 135 in Fig. 1A).

In terms of more specifics, Fig. 1A presents a broad picture road map for a switch fabric embodiment of the invention. (A second, job processing embodiment is shown in Figs. 7A-7B.) In Fig. 1A, a **first set** of *independently-clocked* entities are shown on the left (101), a **second set** of *independently-clocked* entities are shown on the right (105), and a distributed, *variable delay communications fabric* (103) is shown between them.

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The disclosed system of Fig. 1A uses a **handshaking mechanism** comprised of sending requests to potential job performers, receiving responsive grants (or not), sending job input data (ingress payloads) to the granting job performer, and receiving processed data

(egress payloads) from the executing job performer. More specifically, look at dashed box 103 of Fig. 1A. The top 4 horizontal lines of box 103 show the handshaking sequence.

- Line 131a represents the sending of a Request from a source chip to the switch fabric.

- Line 132a represents the sending of a responsive Grant from a member of the switch fabric to the source chip. (This Grant signal contains a first time stamp, GTSa.)

- Line 131b represents the responsive sending of an ingress payload from the Grant-receiving source chip to the grant-providing member of the switch fabric. (This ingress Payload transmission contains a second time stamp, GTSb.)

- Line 132b represents the forwarding (egressing) of a switched payload from the switch fabric to a destination chip, usually different from the payload-sourcing chip.

The four lines do not mandate 4 different wires. Generally there is ingress traffic 133 heading toward the switch fabric 105 and egress traffic 135 going the other way.

That is the ground floor level picture. Things get a bit more complicated though when the switch fabric 105 is a distributed one because different chips within the distributed switch fabric can operate each with its own independent clock. This latter concept is better shown in Fig. 1B by clocks CLKg, CLKh, CLKj, etc. (Fig. 1A also shows the independent clocks at 157, 167 and 177 on the right side.)

Things get even more complicated when the line card layer (101) is a distributed one because different chips within the distributed line card layer can operate each with its own independent clock. This latter concept is shown in Fig. 1B by clocks CLKa, CLKb, CLKc, etc. (Fig. 1A also shows the independent clocks at 117, 127 and 1N7 on the left side.)

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Since the clocks are independent, each can have a slightly different frequency. Over time, one clock can creep ahead of a slower second one. As a result request rates can creep

ahead of grant rates and the requestors can overwhelm the switch fabric. This concept is crudely represented in boxes 108 and 107 at the right side of Fig. 1B.

Aside from the independent clocking aspect of the distributed requestors (ZINC's) and job performers (ZEST's), the system shown in Fig. 1A can have the further complication that transmission time over the interconnect fabric 103 can vary depending on the paths taken by transmitted cells (i.e., ZCells: see Fig. 5A) as they traverse the interconnect. See also the variable transmission latencies depicted in Fig. 2A for ingress line 231 and egress line 238.

The above is a quick, simplified, introduction into what is going on in this application. If anything said in this introduction conflicts with what is said in the specification, or appears to limit the scope of what is said in the specification, then the broader and/or different description in the specification controls. It is roughly 4 years since the specification was written, and initial memory of all details therein may have faded.

Ascertaining the Scope of the Claims

With the above introduction in mind, let us take a look at Claim 1 so we can better ascertain how the claim may be reasonably construed in light of the specification.

The preamble of Claim 1 describes "an independently-clocked job requestor". A packet sourcing chip such as 119 of Fig. 1A can contain such a job requestor.

The preamble of Claim 1 describes "an independently clocked, job processor". A packet switching chip such as 151 of Fig. 1A can contain such a job processor.

The preamble of Claim 1 states that "variable communication latencies may exist between the job requestor and the job processor". The asynchronous line-to-switch interconnect layer 103 of Fig. 1A can cause such variable communication latencies to develop between the line card layer 101 and the switch fabric layer 105. (See again Fig. 2A.)

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Paragraph (a) of Claim 1 describes the "issuing to the job requestor [of] a first time stamp" (emphasis added). Transmission 132a (containing first time stamp GTSa) can satisfy this first step.

Paragraph (b) of Claim 1 describes a step "(b) in response to receipt ... [of] sending ... a combination of job payload data and a second time stamp" [text modified for readability here]. Transmission 131b (containing second time stamp GTSb) can satisfy this second step. Similarly for Paragraph (c) of Claim 1, item 154 can satisfy the step of "storing the received job payload data in the job processor" (emphasis added). Moreover, for Paragraph (d) of Claim 1, control of the switch matrix slice 155 can satisfy the "causing [of] the job processor to process the stored payload data when a time corresponding to the second time stamp occurs within the timing reference frame of the [independently clocked,] job processor" (emphasis added).

Assigning weight to Preamble of Claim

It is well established law that weight must be given to the preamble of a claim if the body of the claim makes antecedent reference to the preamble. See for example, NTP, Inc. v. Research in Motion, LTD __USPQQ2d ___ (Fed. Cir. August 2, 2005) which explains a similar holding in Bell Communications Research, Inc. v. Vitalink Communications Corp., 55 F.3d 615, 620 (Fed. Cir. 1995) ("[W]hen the claim drafter chooses to use both the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects."). "When limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention." Eaton Corp. v. Rockwell Int'l Corp., 323 F.3d 1332, 1339 (Fed. Cir. 2003); see also C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1350 (Fed. Cir. 1998) ("[A] preamble usually does not limit the scope of the claim unless the preamble provides antecedents for ensuing claim terms and limits the claim accordingly.").

Ascertaining the Scope of the Prior Art

It is also well established law that scope and content of the prior art must be properly ascertained (paraphrasing Graham v. John Deere Co., 148 USPQ 459, 467 (SCt. 1966).

A first question presented therefore is: What is Doucer '061 all about?

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A subsidiary question is: Can Doucer '061 be reasonably construed so that Claim 1 reads on the disclosure of Doucer '061 from the view point of one ordinarily skilled in the art?

Of course, Applicant is going to answer, NO.

Here is why.

Broadly, Doucer '061 does not employ a request and grant handshaking system. Electronic search of the Doucer '061 document as stored on the PTO's Internet accessible database on 10/8/2005 shows no occurrence of the string, "request". Electronic search of the Doucer '061 further shows no occurrence of the strings: "grant"; "acknowledge"; "handshake" or "hand shake". These are common terms of art and would be expected to occur within Doucer '061 if Doucer had a request-making and counter-responsive grant-giving mechanism. It does not.

Looking more closely at Doucer '061, it is seen that the Office Action of 8/5/2005 (OA) focused on column 8 of Doucer. Col. 8 describes Figs. 2-3. Let's step back for a moment and look at Doucer Fig. 1. Despite the numerous boxes, what is basically shown in Fig. 1 is a local computer 20, a remote computer 49, and a network coupling 51/52 between the two computers.

Fig. 2 of Doucer '061 shows a one-way, open-loop, data flow within one of the computers (the local or head end computer) as that flow of packets heads out to the other computer via network interface 64. On the left, a group of different packet flows 56 are moving toward a set of "conformers" 58. Each "conformer" associates a specific "conformance time" with each incoming packet 56; where the conformance time is set according to a particular conformance algorithm or set of traffic parameters made unique to each individual packet flow. Then the flows of conformed packets move into respective "shapers" 60. Finally, the shaped packet sequences flow and merge into a sequencer 62. The terms, "conformer" and "shaper" do not appear to be common terms of art. The examiner is correct in understanding that the "conformer" is some sort of time stamping means in that it stamps a respective "conformance time" into association with each passing through packet. But what exactly is a "conformance time"?

This is a good time to step back again and understand the purpose of the "conformance time" and the overall purpose of Doucer '061. The purpose is to assure that a minimum

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packet receipt rate required at the remote destination end (remote computer 49 of Fig. 1) will be met by a packet output rate provided at the source end (local computer 20) of the network.

More specifically, with regard to the local computer 20, Doucer states: "Throughout this application, the PC environment will be assumed though the discussion ..." (col. 1: line 35). Doucer then continues: "[S]treaming data that is communicated from one computer to another such as successive sound or video frames ... **must be processed on a rate basis at the destination node** and that **same rate** should be maintained for packet delivery over the network connection." (1:47, emphasis added). The reason is that; "When quality of service requirements are not met in such an application, [then at the destination end] a jerky or frozen image may result or the picture and sound may appear too unnatural for interaction due to delay. " (2:27, emphasis and bracketed text added).

So Doucer uses various conformance assurance algorithms inside the packet sourcing computer (20) so that: "[O]nce the bandwidth reservations are made [at the source end], the packets may be sent as part of a data stream from the source node to the destination node with the assurance that a certain quality of service will result due to the bandwidth reservation." (2:2).

Doucer uses a factor he calls, the "conformance time" to solve the problem of: "What is needed is a flexible packet scheduling mechanism that allows different algorithms to be supported for each packet flow." (2:36)

Doucer defines each conformer 58 of Fig. 2 as follows: "[A] conformer [component] will generate and assign to each packet in the packet flow at least one **conformance time that signifies the earliest time at which a packet may be sent** while still conforming to the network resource requirements associated with the flow." (Summary 3:15).

One of the conformance algorithms that Doucer supports is: "a token bucket algorithm for setting the conformance time with respect to the sustained data rate and a leaky bucket algorithm that recalculates the conformance time so that the peak data rate may be met." (3:28). There is also a discard test associated with this: "After the generation of the conformance time ..., the discard test is made. Finally, the conformance time is recalculated based on the leaky bucket algorithm and sent down to a shaper component. It is **necessary** to base the discard test upon the **sustained-rate conformance time**, rather than the peak-rate

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conformance time, due to the batch nature of packet processing in the protocol stack in the PC environment. Otherwise, an undue number of packets may be discarded thereby resulting in unacceptable performance characteristics." (3:36-45, emphasis added).

So as can be seen from the above, computation and attachment of the conformance time is followed in Doucer by sending the packet to the "Shaper" 60. The "shaper component [60] is used **to delay** the packets. This will shape the packet traffic so that the packets will be delivered in general around the actual conformance time. Traffic shaping is selectable on a packet flow basis and if it is not performed, the packet is simply passed through the shaper component onto the next processing component." (3:46-53, emphasis and bracketed text added).

Column 8 of Doucer '061 basically repeats the above with reference to details of Figs. 2 and 3.

Failure of the Office Action to make specific Findings of Fact

Especially in complex cases such as the present one, it is the obligation of the PTO to provide the Applicant with sufficiently "useful"" information pursuant to statute (35 USC §132) and rules rather than leaving the Applicant "in a darkroom to shoot arrows at unseen moving targets" in an attempt to defend his patent application (paraphrasing Plager, J. at 24 USPQ2d 1447 in the case of In re Oetiker 24 USPQ2d 1443 (Fed. Cir. 1992)). By way of reference here, 35 USC §132 states:

> (a) Whenever, on examination, any claim for a patent is rejected, or any objection or requirement made, the Director shall notify the applicant thereof, stating the **reasons** for such rejection, or objection or requirement, **together with such information and references** as *may be useful* in judging of the propriety of continuing the prosecution of his application; and if after receiving such notice, the applicant persists in his claim for a patent, with or without amendment, the application shall be re-examined. [emphasis added].

In the present case, Applicant has not been clearly notified as to what specific element of Doucer '061 is considered by the PTO to be the equivalent of the independently-clocked job requestor. Is it the PC-internal, conformer? If so, why is that seen by the ordinary artisan as a job requestor? No "reasons" are given.

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What element of Doucer '061 does the PTO contend to be the independently-clocked, job processor? Is it the PC-internal, shaper? If so, why is that seen by the ordinary artisan as a job processor? No "reasons" are given. How are all the details of Claim 1 met by Doucer '061? For example, what causes the conformers and shapers of Doucer '061 to be independently clocked? Applicant has no idea and will not engage in a blind shooting of arrows at unseen moving targets in a dark room. A prima facie case of unpatentability has not been presented with respect to Claim 1, and for similar reasons with respect to any of the other claims in view of the cited art.

Traverse of Request for New Title

The new title proposed by the PTO at OA page 2 has 9 words. The original title presented by Applicant has 29 words. The PTO makes an unsupported finding that the 29-word original title is not "descriptive". The PTO implies that it's proposed 9-word substitute title is "clearly indicative of the invention to which the claims are directed." Claim 1 uses the past tense term, "scheduled" and not the present tense "Method for Scheduling" that the PTO proposes. It is respectfully submitted that, although well intended, the PTO proposal is not more clearly indicative of the invention. The claims define the claimed subject matter as read in light of the specification. A significant amount of thought went into picking out the title as originally presented. The PTO should reconsider the totality of the situation before trying to insist that Applicant provided a misdescriptive title in place of the original title.

Traverse of Indefiniteness Rejection

No specific basis of rejection is given at OA pages 3-4. Instead the examiner states that a "best effort" was exerted to take meaning out of the claims. The examiner indicates an understanding that there is "scheduling" of packets for transmission at certain time windows. Well, yes and no; but that is not what Claim 1 for example says. The disclosed system can handle ATM traffic (see queues 115, 116 of Fig. 1A) and also other kinds of traffic. A broader description of the system is provided in sister application, 09/847,711 entitled, MULTISERVICE SWITCHING SYSTEM WITH DISTRIBUTED SWITCH FABRIC (underlining added). The "multiservice" part refers to the ability of the switch fabric system to

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handle routing of different kinds of packet traffic, including ATM traffic, which yes, does demand a tight schedule in order to meet QOS requirements. However, the present application is directed at least in part to the expandability (scalability) of a system wherein handshaking occurs between requesting line cards (distributed line cards, optionally on different shelves or daughter boards) and the switch fabric slices (also optionally distributed across different shelves or daughter boards) despite the fact that the line cards and switch slices are distributed and operating on independent clocks and communicating with one another through an interconnect (103) that exhibits variable-latency. It is the asynchronous independently-clocked nature of this distributed system that presents a host of problems. One of the problems is that the time frames inside one or more of the switch fabric components are not the same as the time frames of one or more of the line cards. See again Fig. 1B of the specification. So how does the system assure that payloads will arrive at the right time into the switch matrix intake queues (item 254 of Fig. 2A) with every part of the system potentially running around with its own independent clock? This is neither a trivial problem, nor is the solution a trivial one.

Once again, Applicant fully understands why the examiner may have had a difficult time understanding the present disclosure. It's not rocket science, but it is fairly complex. It is hoped that the informal exchanges with the Examiner and the present response have provided a better understanding.

At page 4 of the OA (end of paragraph 10), the PTO suggests: "It is recommended that the claims be redrafted, clearly indicating the limiting factors and how the scheduling method operates." Applicant respectfully submits that it is not the job of the claims, but rather of the detailed specification to provide descriptions of the various structures and functions. The OA assumes that there is one scheduling algorithm and that this is the gist of the invention so to speak. The OA is wrong on both counts. While Figs. 1A-6 of the application are directed to a case where a switch fabric performs the requested process of routing payload packets from source to destination, application Fig. 7A illustrates another situation where a data processor 750 operating in a clocked domain "D" receives data from independently clocked databases (710 running on clock CLK-A and 720 running on clock CLK-B) and joins the data in unit 753 for subsequent co-processing in unit 754. The specification states in paragraph [0199]:

> An independently-clocked scheduler 740 is further provided for scheduling a time slot within the time domain of processor 750 where the

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> scheduled time slot is one within which corresponding outputs 719 and 729 of the databases are to be joined (753) and optionally further processed (754). Operations of the scheduler 740 are synchronized to a fourth independent clock 747 (CLK C). In an alternate embodiment, the scheduler 740 is integrated with the processor 750 and both are synchronized to a common clock (747 or 757). [Emphasis added.]

Additionally it is made clear to the left of item 703 and to the right of item 706 in Fig. 7A that there are other schedulers and other processes. Paragraph [0210] states:

> As indicated by dashed boxes 703 and 706, the first and second database computers, 710 and 720, may constitute distributively shared resources that serve more than just scheduler 740 and its related processor 750. Different, optionally-variable latencies may be associated with the interconnects 703, 706 to those other schedulers and processors (not shown). Each pair of scheduler (740) and its related processor (750) may have a different RTA' value [Roundtrip Adjustment Factor] associated with it. [Emphasis and bracketed text added.]

The above demonstrates that there is no one scheduler and that the scheduling algorithm is not per se at the heart of the invention. Fig. 7B better shows that one embodiment of the invention includes a statically-slowed job processor 780 and a dynamically-slowed requestor (customer) 790. The dynamically-slowed requestor 790 sends empty request packets 778 when its token-based, rate control algorithm 770 determines that the job processor may be receiving requests at a faster rate than it can handle. The details are in the specification. Once again, if anything said here in this rough explanation conflicts with what is said in the specification, or appears to limit the scope of what is said in the specification, then the broader and/or different description in the specification controls. It is roughly 4 years since the specification was written, and initial memory of all details therein may have faded.

With regard to Claim 2, the PTO asserts at OA page 5, paragraph 14, that requests and grants are described by Doucer '061. Applicant respectfully disputes this finding of fact. There is no request/grant handshake in Doucer '061.

With regard to Claim 3, the PTO has no basis in fact for asserting that Doucer '061 teaches sequence indicators.

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With regard to Claim 4, the PTO has no basis in fact for asserting that Doucer '061 teaches scheduled time slots within respective timing reference frames of respective job processors.

With regard to the rest of the claims, the PTO is seen as making yet further unsupported findings. It is not understood what the OA refers to at page 8 with regard to "inherent" ECC due to dealing with "conformance". Claim 25 belongs to the dependency chain of claims 22/24/25. It cannot be arbitrarily disassociated from that chain.

It is respectfully submitted that there have been errors in the fact finding process and errors in the claim interpretation process. Reconsideration is respectfully requested. Given that all outstanding rejections are founded on the above-identified, incorrect reading of Doucer, they should all be withdrawn at least for that reason alone.

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CONCLUSION

In light of the foregoing, Applicant respectfully requests that the outstanding rejections be withdrawn. Should any other action be contemplated by the Examiner, it is respectfully requested that he contacts the undersigned at (408) 392-9250 to discuss the application.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-2257 for any matter in connection with this response, including any fee for extension of time and/or fee for additional claims, which may be required.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on __October 28_, 2005.

[signature] 10-28-2005

Attorney for Applicant(s) Date of Signature

Respectfully submitted,

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